WHAT IS CLAIMED IS:

1. A substrate for mounting at least one die within an integrated circuit, comprising:

a dielectric layer defining a first surface of the substrate and having channels therein for addition of circuit material, the channels having sides extending to a plane defining the first surface of the substrate and having a bottom beneath the plane defining the first surface of the substrate, and wherein the channels include at least one land area formed from multiple channels within the substrate; and

circuit material deposited within the channels for forming an electrical connection between electrical contacts of the at least one die and electrical terminal lands on the substrate, and wherein the at least one land area forms a shape having non-channel regions within a perimeter of the land area, whereby plating and etching current density of the circuit material deposited within the at least one land area is reduced and dimpling of the circuit material within the at least one land area is reduced or eliminated.

2. The substrate of Claim 1, wherein the at least one land area is a grid formed from multiple channels within the perimeter of the at least one land area, whereby the circuit material deposited within the perimeter of the at least one land area forms a grid of conductive material.

3. The substrate of Claim 2, wherein the multiple channels comprise:

a first plurality of parallel channels;

a second plurality of parallel channels orthogonal to the first plurality of parallel channels in a plane defined by the first surface of the substrate.

4. The substrate of Claim 2, wherein the perimeter of the at least one land area is a rectangle, whereby a mounting land for a surface-mount component is provided by the circuit material deposited within the at least one land area.

5. The substrate circuit of Claim 2, wherein the perimeter of the at least one land area is a circle, whereby a land for a solderball is provided by the circuit material deposited within the at least one land area.

6. The substrate of Claim 1, wherein the at least one land area is multiple channel sub-areas having a common predetermined geometric shape and disposed radially around a center of the at least one land area, and further comprising interconnect channels interconnecting the multiple channel sub-areas, whereby the circuit material deposited within the perimeter of the at least one land area forms a circular pattern having voids between the sub-areas.

7. The substrate of Claim 6, wherein one of the sub-areas is a first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are circular areas radially disposed around the first circular sub-area.

8. The substrate of Claim 6, wherein one of the sub-areas is a first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are annular segments radially disposed around the first circular sub-area.

9. An integrated circuit, comprising:

a substrate having channels therein for addition of circuit material, the channels having sides extending to a plane defining a first surface of the substrate and a bottom beneath the plane defining the first surface of the substrate, and wherein the channels include at least one land area formed from multiple channels within the substrate;

a die mounted to the substrate;

a plurality of electrical terminals mounted to the substrate for connecting the die to external circuits; and

circuit material deposited within the channels for forming an electrical connection between die electrical contacts of the die and the electrical terminals, and wherein the at least one land area forms a shape having non-channel regions within a perimeter of the land area whereby plating and etching current density of the circuit material deposited within the at least one land area is reduced and dimpling of the circuit material within the at least one land area is reduced or eliminated.

10. The integrated circuit of Claim 1, wherein the at least one land area is a grid formed from multiple channels within the perimeter of the at least one land area, whereby the circuit material deposited within the perimeter of the at least one land area forms a grid of conductive material.

11. The integrated circuit of Claim 10, wherein the multiple channels comprise:

a first plurality of parallel channels;

a second plurality of parallel channels orthogonal to the first plurality of parallel channels in a plane defined by the first surface of the substrate.

12. The integrated circuit of Claim 10, wherein the perimeter of the at least one land area is a rectangle, whereby a mounting land for a surface-mount component is provided by the circuit material deposited within the at least one land area.

13. The integrated circuit of Claim 10, wherein the perimeter of the at least one land area is a circle, whereby a land for a solderball is provided by the circuit material deposited within the at least one land area.

14. The integrated circuit of Claim 1, wherein the at least one land area is multiple channel sub-areas having a common predetermined geometric shape and disposed radially around a center of the at least one land area, and further comprising interconnect channels interconnecting the multiple channel sub-areas, whereby the circuit material deposited within the perimeter of the at least one land area forms a circular pattern having voids between the sub-areas.

15. The integrated circuit of Claim 14, wherein one of the sub-areas is a first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are circular areas radially disposed around the first circular sub-area.

16. The integrated circuit of Claim 14, wherein one of the sub-areas is a first circular sub-area disposed at the center of the at least one land area and the remaining sub-areas are annular segments radially disposed around the first circular sub-area.

17. A substrate for mounting at least one die within an integrated circuit, comprising:

a dielectric layer defining a first surface of the substrate and having channels therein for addition of circuit material, the channels having sides extending to a plane defining the first surface of the substrate and having a bottom beneath the plane defining the first surface of the substrate; and

circuit material deposited within the channels for forming an electrical connection between electrical contacts of the at least one die and electrical terminal lands on the substrate; and, wherein the dielectric layer further includes means for reducing a plating/etching current density of the circuit material deposited within at least one land area of the circuit material, whereby dimpling of the circuit material within the at least one land area is reduced or eliminated.

18. The substrate of Claim 17, wherein the reducing means further comprises means for reducing a plating area of the at least one land area, whereby plating cost of the substrate is reduced.

19. A method of manufacturing an integrated circuit, the method comprising:

forming channels within a dielectric layer defining a first surface of a substrate, the channels having sides extending to a plane defining the first surface of the substrate and having a bottom beneath the plane defining the first surface of the substrate, the channels further including at least one land area formed from multiple channels within the substrate, and wherein the at least one land area forms a shape having non-channel regions within a perimeter of the land area;

depositing conductive material completely filling the channels and extending over the first surface of the substrate; and

etching the deposited conductive material, whereby conductive patterns are formed from the conductive material deposited in the channels and at least one land is formed from conductive material deposited in the at least one land area, whereby the conductive material in the at least one land area is not substantially dimpled by the etching due to a reduction of current density at the at least one land area.

20. The method of Claim 19, wherein the forming is performed by laser ablating the dielectric layer.